AP2H-MM85xxMC

QSFP56 200Gb/s 850nm 1~100m AOC Transceiver

PRODUCT FEATURES

- Compliant with IEEE Std 802.3bs, IEEE Std 802.3cm
- Compliant with 200G-SR4 optical specifications
- Compliant with SFF-8679
- Compliant with CMIS4.0 Management interface specificati
- 4x53.125Gb/s electrical interface (200GAUI-4)
- Reach up to 70m on MMF(OM3)
- Reach up to 100m on MMF(OM4)
- Single +3.3V power supply
- Case temperature range: 0 ~ +70℃
- Maximum power consumption 5W
- Single MPO12 connector
- RoHS complaint

APPLICATIONS

- 200GBASE-SR4 200G Ethernet
- Data center interconnection

PRODUCT DESCRIPTION

Photonics Valley's 200G QSFP56 AOC is a 4×50Gbps multi-mode fiber, hot pluggable optical transceiver.

The module integrates four parallel lanes with baud rate at 26.5625GBd each lane. It can transmit up to 70 m on fiber OM3 fiber or 100 m on OM4 fiber with FEC.

Ordering information

Part Number	Reach	Temp	RoHS
AP2H-MM8501MC	1m	0 ~ 70 °C	Compliant
AP2H-MM8502MC	2m	0 ~ 70 °C	Compliant
AP2H-MM8503MC	3m	0 ~ 70 °C	Compliant
AP2H-MM8505MC	5m	0 ~ 70 °C	Compliant
AP2H-MM8507MC	7m	0 ~ 70 °C	Compliant
AP2H-MM8510MC	10m	0 ~ 70 °C	Compliant
AP2H-MM8520MC	20m	0 ~ 70 °C	Compliant
AP2H-MM8530MC	30m	0 ~ 70 °C	Compliant
AP2H-MM8550MC	50m	0 ~ 70 °C	Compliant
AP2H-MM8570MC	70m	0 ~ 70 °C	Compliant

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	+85	°C
Operating Humidity	RH	10	90	%
Supply Voltage	Vcc	0	4	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Supply Voltage	Vcc	3.14	3.3	3.46	V
Pre-FEC BER				2.4×10^{-4}	
Damage Threshold	Pin	4.5			
Power Consumption	P_{Diss}			5.0	W
Fiber Length onOM3				70	m
Fiber Length on OM4				100	m

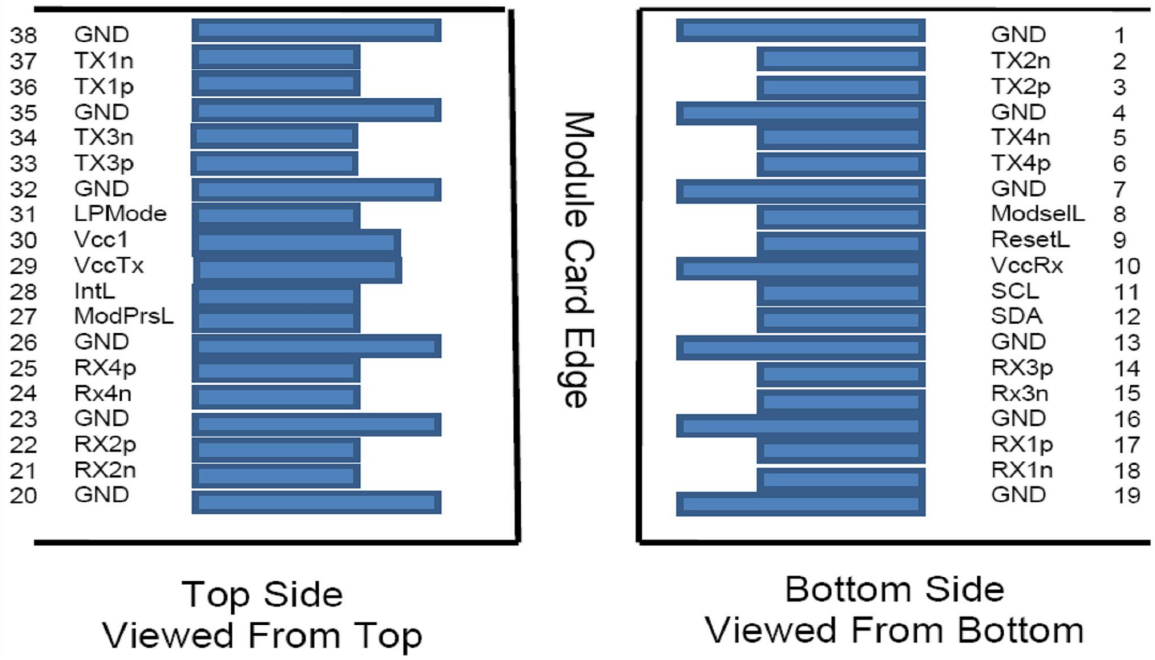
Table3. Transmitter Optical Specifications

Transmitter Parameter	Min	Typical	Max	Units
Signaling Rate, each lane		26.5625 ± 100 ppm		GBd
Center Wavelength Range	840	850	860	nm
Modulation Format		PAM4		
Average launch Power per lane	-6.5		4	dBm
RMS spectral width			0.6	nm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane	-4.5		3	dBm
Average Launch Power per Lane @ TX Off State			-30	dBm
Launch Power in OMAouter minus TDECQ, each Lane	-5.9			dBm
Transmitter and Dispersion Eye Closure for PAM4, each Lane			4.5	dB
Extinction Ratio	3			dB
Optical Return Loss Tolerance			12	dB
Encircled flux at 4.5um			30	%
Encircled flux at 19um	86			%

Table4. Receiver Optical Specifications

Receiver Parameter	Min	Typical	Max	Units
Signaling Rate, each lane		26.5625 ± 100 ppm		
Lane Wavelength Range	840	850	860	nm
Modulation Format				
Damage Threshold	5			dBm
Average Receive Power, each lane	-8.4		4	dBm
Receiver Power, each lane (OMA)			3	dBm
Receiver Reflectance			-12	dB
Receiver sensitivity(OMA_{outer})each lane(SECQ=1.4dB)			-6.5	dBm
Stressed Receiver Sensitivity (OMA_{outer}), each lane			-3.4	dBm
Stressed Conditions for Stress Receiver Sensitivity				
Stressed Eye Closure for PAM4 (SECQ),Lane under Test		4.5		dB
SECQ-10log10(Ceq),each lane			4.5	
OMA_{outer} of each Aggressor Lane		3.0		dBm

Pin Description

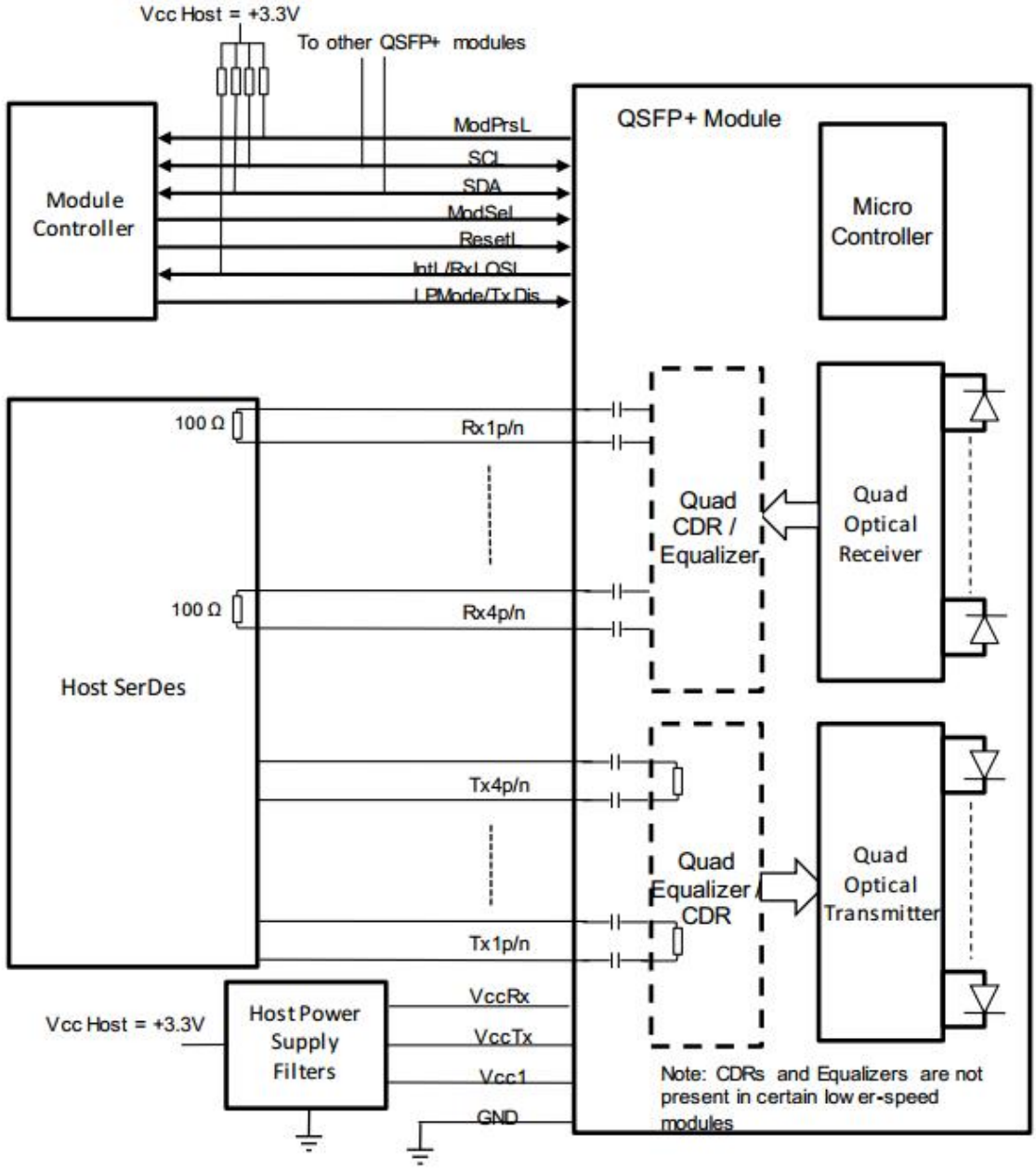


QSFP compliant 38-pin connector

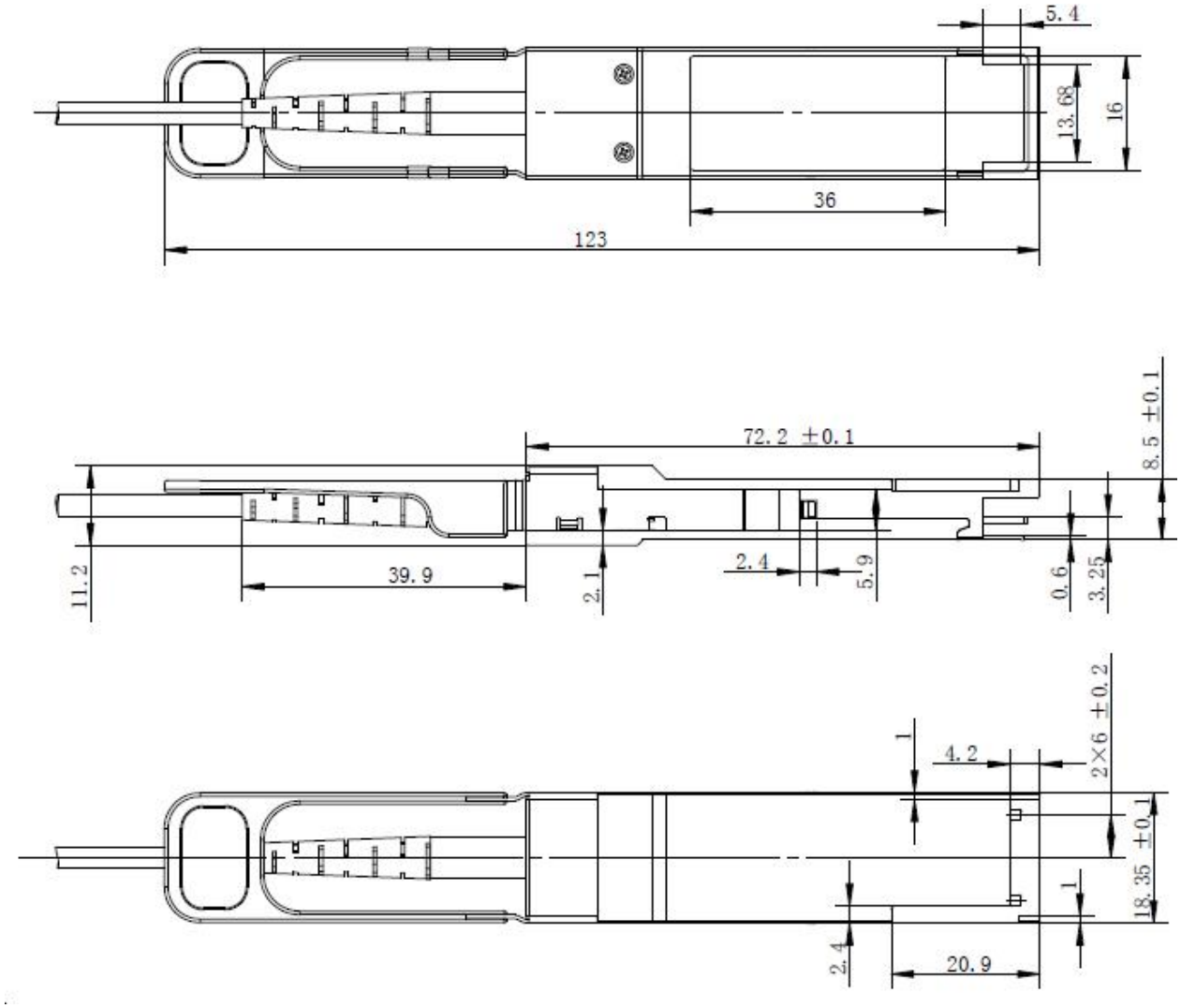
QSFP Transceiver Pinout

Pin No.	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1
2	CML-I	TX2n	Transmitted Inverted Data Input	3
3	CML-I	TX2p	Transmitted Non-Inverted Data Input	3
4		GND	Ground	1
5	CML-I	TX4n	Transmitted Inverted Data Input	3
6	CML-I	TX4p	Transmitted Non-Inverted Data Input	3
7		GND	Ground	1
8	LVTTL-I	ModSeil	Module Select	3
9	LVTTL-I	ResetL	Module Reset	3
10		Vcc Rx	+3.3 VDC Receiver Power Supply	2
11	LVCMOS-I/O	SCL	Serial Clock for I2C Interface	3
12	LVCMOS-I/O	SDA	Serial Data for I2C Interface	3
13		GND	Ground	1
14	CML-O	RX3p	Receiver Non-Inverted Data Output	3
15	CML-O	RX3n	Receiver Inverted Data Output	3
16		GND	Ground	1
17	CML-O	RX1p	Receiver Non-Inverted Data Output	3
18	CML-O	RX1n	Receiver Inverted Data Output	3
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	RX2n	Receiver Inverted Data Output	3
22	CML-O	RX2p	Receiver Non-Inverted Data Output	3
23		GND	Ground	1
24	CML-O	RX4n	Receiver Inverted Data Output	3
25	CML-O	RX4p	Receiver Non-Inverted Data Output	3
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	3
28	LVTTL-O	IntL	Interrupt	3
29		Vcc Tx	+3.3 VDC Transmitter Power Supply	2
30		Vcc1	+3.3 VDC Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	3
32		GND	Ground	1
33	CML-I	TX3p	Transmitted Non-Inverted Data Input	3
34	CML-I	TX3n	Transmitted Inverted Data Input	3
35		GND	Ground	1
36	CML-I	TX1p	Transmitted Non-Inverted Data Input	3
37	CML-I	TX1n	Transmitted Inverted Data Input	3
38		GND	Ground	1

Module Block Diagram



Mechanical Dimensions



Regulatory Compliance

Agency	Standard	Certificate /Comments
CE-EMC	EN 55032: 2015	17706703 003
	EN 55024: 2010+A1	
REACH	REACH SVHC 197	68.420.19.0344.01
FCC	FCC Rules and Regulations Part 15 Subpart B Class B	MTi190422E141C
RoHS	2011/65/EU and amendment (EU) 2015/863	68.420.17.1030.01